RISC PC

Data Sheet 4
Acorn Floating Point Accelerator (FPA11)

April 1994

FPA11 is a floating point accelerator suitable for use with the ARM700 CPU, due to be introduced into the Acorn Risc PC later in the year. It uses a combination of silicon and software to deliver a cost-effective level of performance combined with low power consumption. The combination of FPA11 hardware and support software provides an IEEE 754-1985 conformant floating point system.

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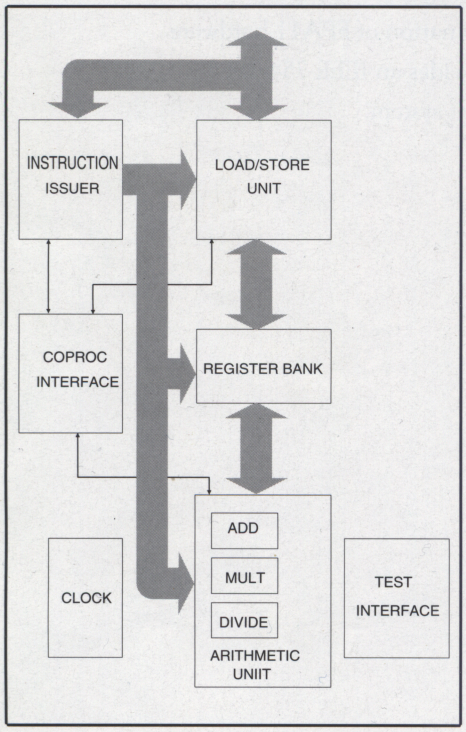
The FPA processor has a peak throughput of up to 5 MFLOPS (Millions of FLoating point Operations Per Second) at 25MHz and achieves an average throughput in excess of 3 MFLOPS for a range of calculations.

Applications which make use of the RISC OS Floating Point Emulator automatically use the FPA chip once installed, increasing floating point performance by as much as a factor of 50. Computationally intensive applications that benefit from the performance increase typically include spreadsheets, finite element analysis, CAD, image analysis, modelling and vector graphics.



The design of FPA11 is based upon an 81-bit internal datapath, with autonomous load/store and arithmetic units which can operate concurrently. Single-, double- and extended-precision IEEE formats are all supported. FPA11 is interfaced to the ARM CPU over a simple, high-performance co-processor bus. The ARM instruction pipeline is mirrored in FPA11 so that floating point instructions can be executed directly with minimum communication overhead. Pipelining, concurrent execution units and speculative execution are all employed to improve performance without significantly impacting power consumption.

A RISC approach has been taken in selecting the floating point instructions which are implemented in hardware, and those which are handled by support software. The FPA11 instruction repertoire includes the basic operations, plus compare, absolute value, round to integral value and floating-point to integer and integer to floating-point conversions. In addition, only normalised operands and zeros are handled in hardware; operations on denormalised numbers, infinities and NaNs are handled by the support code.

Only the inexact exception is dealt with by hardware; all other exceptions cause the software support code to be called, whether or not the associated trap is enabled. This approach has helped to minimise the die size whilst having a negligible effect on performance in most applications.

The chip is implemented in 0.8 micron double-level metal CMOS, contains 130,000 transistors and is packaged in a 68-pin PLCC package. It fits into a socket on the ARM 700 processor PCB.

United Kingdom
Acorn Computers Limited
Acorn House
Vision Park
Histon
Cambridge CB4 4AE

Telephone (0223) 254254
Int +44 223 254 254
Fax (0223) 254262

Australia
Acorn Computers
Australia Pty Ltd
29 Cromwell Street
Collingwood
Victoria 3066

Telephone: (03) 419 3033
Int +61 3419 3033
Fax (03) 419 2892

Australia
Acorn Computers
Australia Pty Ltd
Unit 7, 190 George Street
Parramatta
New South Wales 2150

Telephone (02) 891 6555
Int +61 2891 6555
Fax: (02) 635 9641

Germany
Acorn Computers GmbH
Jürgensplatz 36-38
40219 Düsseldorf

Telephone (0211) 308 494
Int +49 211 308 494
Fax (0211) 394386

New Zealand
Acorn Computers
New Zealand Ltd
1 Ngaire Avenue
PO Box 26 - 287
Epsom, Auckland 3

Telephone (09) 520 4049
Int +64 9520 4049
Fax: (09) 520 3321

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